



A novel square wave generator based on the translinear circuit scheme of second generation current controlled current conveyor-CCCII

Umar Mohammad¹  · Mohd Yusuf Yasin² · Romana Yousof¹ · Imtiyaz Anwar¹

© Springer Nature Switzerland AG 2019

Abstract

A robust square wave generator employing a sole capacitor and two resistors has been presented in this study. Low power as well as popular translinear circuit scheme of Second generation current controlled current conveyor-CCCII has been taken as an active element to implement the proposed square wave generator. CCCII inhibits promising features like availability of three mutually independently and electronically adjustable parameters corresponding transconductance (g_m), intrinsic resistance (r) of the current input terminal and current gain between two terminals) that are very prevalent for control applications accepted currently. The operating frequency of the proposed model has been analyzed with respect to the passive components present there, with no exposure of output signals to the thermal voltage (V_T). Electrical/Device properties (like Noise, Threshold, area etc.) of the proposed circuit have also been discussed in this work. The simulation work was carried out on *Synopsis Hspice tool (v-2008.03)* from *Avant*. Satisfying results with anticipation of theoretical and simulated results, including precision (*consistency assessment*) with Pareto analysis (*1st order Best Test flavored by Decision making analysis*) were observed during the study. The 45 nm *BSIM CMOS* modelling parameters were adopted to prove the theory. The elementary purpose of using such parameters is to maximize the circuit drive and lowering the leakage current. Another purpose of using these modelling parameters is to enhance the realization of the proposed circuit in the form of chip die and further get it fabricated in custom Integrated circuit(IC) form, from a Standard local foundry. Maximum power consumption of the circuit is 600 μ W, with ± 1 V rail to rail operating voltages.

Keywords Square wave generators · CCCII based novel MOS devices · Monte Carlo analysis · Voltage and current mode circuits · Low power and low voltage CMOS circuits

1 Introduction

In the recent years, the digital systems have maintained strong dominance over the traditional analog systems due to their outstanding features and characteristics [1–6]. But still analog devices/circuits can't be overruled or neglected, for the reason of their long term consistency in various engineering fields, by the advantage of

their promising features. Advancements in both the fields have framed and shaped the fourth industrial revolution. Likely, square wave generator is the basic building block of many signal processing elements like A/D and D/A converters, applied electronics and instrumentation [7–12]. In literature, a number of square wave generators have been presented, that differ among each other by one or the other feature. Multiple active devices have been utilized

This work was supported by the Special Assistance Program, SAP, at the Islamic University of Science & Technology-IUST, Awantipora, Kashmir, India for the up gradation and improvement of the Institutional Technical education and research quality.

✉ Umar Mohammad, umarnaik@iul.ac.in; Mohd Yusuf Yasin, myyasin@iul.ac.in; Romana Yousof, romana.yousuf@islamicuniversity.edu.in; Imtiyaz Anwar, imtiyaz.anwar@islamicuniversity.edu.in | ¹Electronics Engineering Department, Islamic University of Science and Technology, Awantipora, Kashmir 192122, India. ²Department of Electronics and Communication Engineering, Integral University Lucknow, Lucknow 226026, India.

SN Applied Sciences (2019) 1:587 | <https://doi.org/10.1007/s42452-019-0608-z>

Received: 23 February 2019 / Accepted: 13 May 2019 / Published online: 18 May 2019

to present the wave generator (C.L. Hou et al. used OTRA) [31], (Pal, D et al. used CCII) [19], (Silapan et al. used MO-CCCDTA) [34], (Sotner, R et al. used ZC-CG-VDCC) [36]. In the paper, we are implementing the square wave generator using the translinear circuit scheme of CCCII. Dominant low power, low voltage devices with full availability of full bandwidth (λ) are expected to ascend using CCCII schemes [13–20]. A detailed Analytical outlook of the pros and cons of the previous and present literature is also discussed in this paper. Fourier components of the voltage (V) at the output node with signal components like frequency (ν), phase(Φ), normalized phase etc. through the reference of Total harmonic distortion (THD) and DC components have also been presented here. Active elements find applications in the field of signal generation, such as controllability of oscillation frequency, control of output amplitudes, duty cycle etc. [18–21].

1.1 Literature review

In literature, we came across different varieties of square-wave generator circuits based on multiple active elements. A detailed comparative summary has been kept in the Table 1 of this study. However, the basic overview of literature present relating the proposed circuit/waveform generators is below.

1. In [29], square wave generator employing two CCII and five passive elements has been reported. Circuit has been verified through simulation and practically using Spice level 1 transistor parameters and AD844AN IC respectively. Maximum range of the tunable frequency has been found 300 kHz. Power consumption of the circuit is 16.83 mW.
2. C.L. Hou et al. in [32] [33] have presented square/triangular wave generator with switch controllable OTRA's. The feasibility of these OTRA's have been verified using commercial AD844AN IC. This study has mainly focused on the practical demonstration of the waveform generators. Silapan et al. [34] have used MO-CCCDTA as an active device to enhance the realization of Schmitt triggers. Bipolar PNP and NPN Pspice transistor models were used to complete the verification purposes. A total of 27 transistors were used to complete the circuit. Moreover multiple devices like AD844AN and LM13600 N have been used to make the possible implementation of the proposed circuits. Enough simulation and calculations are reported in the study. Power consumption of one of the circuits is 235 μ W.
3. In [35], Sotner, R et al. have presented ZC-CG-VDCC as an active element to implement the fully fledged functional generator using both current and voltage signals. Circuit topology of the active element was completed with 52 MOS transistors using 0.18 μ m CMOS technology. Practical implementation of the design has also been reported using diamond transistors, buffer models-BUF634/OPA660/860 and two resistors. Backing this work, Sotner, R et al. in [36], [37], [38] presented DT-VCA, DO-FB-VDBA & CG-CDVA as active elements to (triangular/squarewave) waveform generators. Possible implementation in simulation and on practical hands have been done greatly. Frequent use of diamond transistor has been done by the authors. Theoretical fitting in these papers is presented greatly. In [39], [40] Srinivasulu, A et al. proposed waveform generators using CCII practically as well as through simulation. Reportedly Cadence Tools were used to simulate the circuit presented at [39] in CMOS micrometer technology, however, at [40] practical implementation of the proposed theory was illustrated using commercially available AD844AN IC's.
4. In [41], [46] Siripruchyanun, M et al. proposed waveform generators using OTA and MO-VDTA. Pspice has been used to simulate the circuit presented in the above cited literature. [41] has reportedly enough application part exceeding square wave generation. BJT transistors has been used to prove the proposed theory. In [46], number of BJT transistors have been increased up to 36 and has been made essential for square/triangular waveform generation. Total Power consumption of the proposed circuit in the study is reported 14.3 mW. In [42] Hung-Chun Chien proposed waveform generators DVCC. This paper presents a voltage-controlled dual slope operation square/triangular wave generator circuits. Various other applications based on multiple differential voltage current conveyors has been reported by the authors. Some practical simulations and verifications have also been proposed in the study. Overall power consumption of the circuit has been reported 763 mW.
5. In [43], Vijay et al. have proposed squarewave generator using Second-Generation Differential Current Conveyor DCCII. Simulation of the circuit was done using cadence systems implying 180 nm gpdk parameters. In addition, hardware realization has also been reported using AD844AN. In [45, 47, 48] chattervedi et al. have proposed multi output active devices MO-DXCCTA, MO-CIDITA for advanced square/triangular waveform generation. Reportedly in the particular literature, few hardware implementation have been done using the commercially available IC's AD844AN and LM13700. Satisfying cooperation of theoretical and practical outputs have been found. Probably, [48] is the only study that has proposed Schmitt trigger without any passive element. Various other features like high frequency,

Table 1 Comparison of the state of art-square wave generator technologies

Reference	Active element	No of active elements	No of passive elements	Grounded capacitor (s)	Grounded resistor (s)	Hardware implemented	Transistor type/IC used	Technology node/Models	Ib/Vcc
C.L. Hou et al. [33]	OTRA	1	4	No	No	Yes	AD844AN	Not applicable	N.A/15 V
C.L. Hou et al. [32]	OTRA	2	4	No	No	Yes	AD844AN	Not applicable	0.9 mA/5 V
Pal D et al. [29]	CCII	2	5	Yes	Yes	Yes	AD844AN	Spice level 1	5–10 V
Silapan et al. [34]	MO-CCCDTA	2	1	Yes	No	Yes	BJT	μM	1.5 V
Sotner R et al. [35]	ZC-CG-VDCC	1	4	Yes	Yes	Yes	MOSFET	0.18 μM	1 V
Sotner R et al. [36]	DT-VCA	3	2	Yes	No	Yes	VCA610, OPA860/660	–	5 V
Sotner R et al. [37]	DO-FB-VDBA	2	3	Yes	Yes	Yes	MOSFET	0.18 μM	50 μA /1.2 V
Sotner R et al. [38]	CG-CDVA	1	2	Yes	No	No	EL2082	Macro models	5 V
Srinivasulu A et al. [39]	CCII	3	7	Yes	Yes	Yes	MOSFET	0.6 μM	6 V
Srinivasulu A et al. [40]	CCII	3	7	Yes	Yes	Yes	AD844AN	Spice model	7 V
Siripruchyanun M et al. [41]	OTA, MO-VDTA	3	3	Yes	Yes	Yes	BJT	Pspice model/ μM	5 V
Chien et al. [42]	DVCC	2	4	Yes	Yes	Yes	AD844AN	Spice Model	–
Vijay et al. [43]	DCCII	1	3	Yes	Yes	Yes	MOSFET	180 nm	2.5 V
Chattervedi et al. [45, 47–50]	DXCCTA/MO-CIDITA	7	22	Yes	Yes	Yes	AD844AN, LM13700	μM /90 nm	–
Ranjan et al. [51]	FTFN	1	2/3/8/10	Yes	Yes	Yes	AD844AN	μM	1.65 V
PROPOSED (Fig. 3)	CCCII	1	2	Yes	Yes	No	MOSFET	45 nm	8 μA /1 V

OTRA Operational trans resistance amplifier

MO-CCCDTA Multiple-output current controlled current differencing transconductance amplifier

ZC-CG-VDCC z-copy controlled-gain voltage differencing current conveyor

DT-VCA Dual transistor voltage controlled amplifier

DO-FB-VDBA Dual output fully balanced-voltage differencing buffer amplifier

CG-CDVA controlled gain current and differential voltage amplifier

CCII Second generation current conveyor

OTA Operational transducer amplifier

DVCC Differential voltage current conveyor

DCCII Second generation differential current conveyor

DXCCTA Dual-X current conveyor transconductance amplifier

MO-VDTA Multi output voltage differencing transconductance amplifier

CCCII Second generation current controlled current conveyor

controllable duty cycle have also been found in the above literature.

- Ranjan et al. in [51] have presented FTFN based Schmitt trigger enlightening the behaviors of square and triangular waveform generation. Pulse width modulation scheme has been used to enhance the realization of the proposed circuitry. Micrometer technology in Pspice tool has been used for the realization of the circuit. Finally hardware implementation has been done using AD844IC. Power Consumption has been figured at 2.4 mW in the study.

While concluding the literature and revealing the post justification, excellence and the commensurate advantages of the proposed design, fewer thing can be settled down finally. Firstly an ultimate low power circuit, implemented using the translinear circuit scheme of second generation current conveyor-CCII has been presented. Which according to the author’s best knowledge isn’t available yet in the literature present. Furthermore, proposed Circuit has lesser complexity in terms of design and component requirement. In standings with the comparative operating frequency, CCII based squarewave generator is expected to work in megahertz range (MHz). Higher slew rate in Gigahertz (GHz) has been found, during the simulation study of the circuit. Finally, a good handoff of theoretical and practical results was seen in the study.

2 Cccii Design, Non Idealities And Considerations

The scheme, we have adopted in the second generation current conveyor is the current mirror based translinear circuit (CCCII+) [13] shown below in Fig. 1. The advantage of using this circuit scheme is that it is fully balanced. The intrinsic resistance in this type can be balanced by tuning the biasing current I_b .

The matrix representation of CCCII is below;

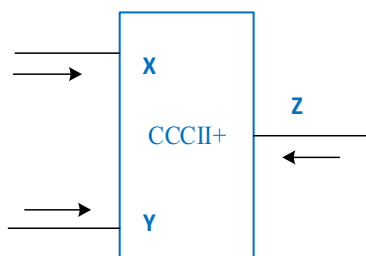


Fig. 1 General representation of CCCII+

From the above matrix as shown in Fig. 2, we can conclude the following things relating the operation of CCCII ±.

$$I_y = 0 \tag{1}$$

$$V_x = V_y + I_x \cdot R_x \tag{2}$$

$$I_{z+} = +I_x \tag{3}$$

$$I_{z-} = -I_x \tag{4}$$

$$\text{Resistance at } x = R_x = \frac{1}{2gm} = \frac{1}{\sqrt{8\beta_n}} I_b \tag{5}$$

where $\beta_n = \mu_n C_{ox} \cdot \frac{W}{L}$

The above equations are well defined from the above matrix in Fig. 2, in which we have, I_y is the node current at Port Y. V_x refers to voltage at node X. V_y is the voltage at node Y. I_z and V_z are the current and Voltages at the node Z respectively. Lastly, R_x is the intrinsic resistance of the translinear circuit. R_x present at port X depends inversely on bias current (IB). The parasitic resistance RX of terminal X is proportional to $1/I_b$ for BJT realizations and inversely proportional to the square root of the bias current for CMOS realization [56] [57]. The Limitations of the CCII enhanced by *Fabre* resulted the new the new device termed as Current controlled current conveyor-CCCII. Inclusion of R_x was shown in the particular device, in order to balance the adjustment of the voltage relationship between node X and node Y, thereby imparting tunability to the device.

Some of the promising features of the CCCII are viz. [22–26]

- Greater Linearity and Current mode Applicability.
- Availability of full bandwidth.
- Auto balancing at higher temperatures.
- Low power & low voltage.

$$\begin{bmatrix} V_x \\ I_y \\ I_z \end{bmatrix} = \begin{bmatrix} R_x & 1 & 0 \\ 0 & 0 & 0 \\ \pm 1 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_x \\ V_y \\ V_z \end{bmatrix}$$

Fig. 2 Matrix representation of CCCII±

3 Proposed and implemented square wave generator

In literature a Variety of circuits quoting reference of square wave generator are available. Few circuits employing CCII [39, 40] as an active device are available. But no such circuit with the translinear circuit scheme of CCCII is available yet. CCCII is expected to enhance the features of the existing literature, because of its dominant features as described above. The literature available has been compiled in the table below.

Figure 3 shows the presented square wave generator circuit. One CCCII+, one capacitor (C), and only two resistors (R₁ and R₂) have been used to implement the circuit. Translinear circuit topology used to drive CCCII+ has been put forth here for the readers.

Captivating CCCII+ as an active principal component and casually joined passive components fashioned a novel square wave generator is shown in Fig. 4, with a single capacitor and two resistances. The Parasitic elements can be tuned to obtain the self-satisfying (*commercially needed for IoT and Cognitive radio*) simulation results.

Considering the ideal input/output terminal characteristics of the CCCII+ documented in Figs. 1, 2, 3 and 4 and Eqs. (1–5). Referring to the notations as shown in Fig. 3 and for ideal CCCII, $i_y = 0 : v_x = v_y + i_x \cdot r_x : i_z^+ = +i_x : i_z^- = -i_x$ and $v_x = v_y$ therefore, i_x flows out of the node X as shown in Fig. 3.

A detailed analysis of the Time period can be investigated from the desired corresponding specimen waveform (provided in Fig. 5) of the proposed circuit.

From the Fig. 5, we have two possible saturation levels pointed as L+ and L- for the output voltage V_o. Individual Steady state operations can be made for the charging as well as the discharging mode of the capacitor. Alternate

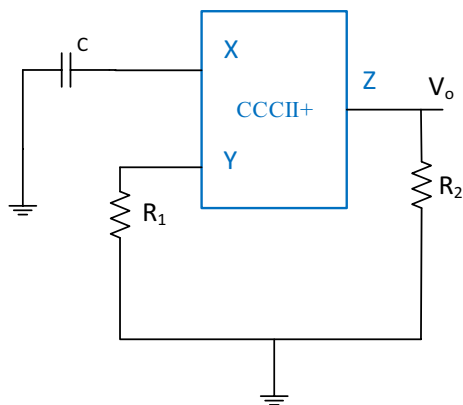


Fig. 3 Proposed circuit of square wave generator

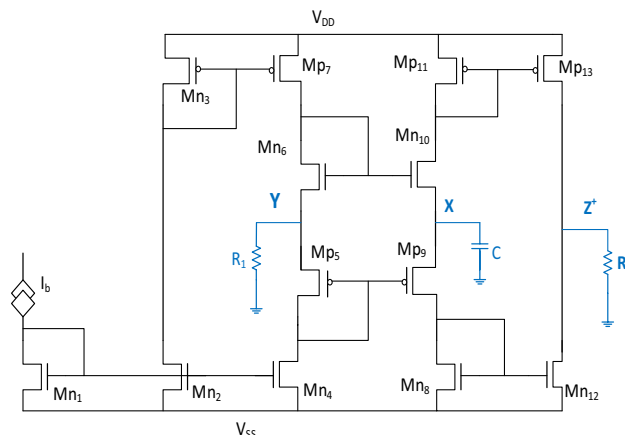


Fig. 4 Proposed circuit implemented using CMOS translinear circuit topology

standard equations presented in the literature [44], [43] can also be followed to sum up the circuit description. Theoretical calculations based on the commensurate observations from Fig. 5 leads us to reveal the probable equations for the time period.

$$V_{out} = V_x \cdot R_2/R_1$$

Now, the Standard charging equation for a Capacitor can be written as;

$$q = CV (1 - e^{-t/RC}) + q_0 \cdot e^{-t/RC} \tag{6}$$

Further, few conclusions can be made for the rising waveform viz: ($V_{c(t)} = \lambda \cdot V_{out}; V_{TL} = -\lambda \cdot V_{DD}; V_{TH} = V_{DD}$) Hence Eq. 6, can be written as;

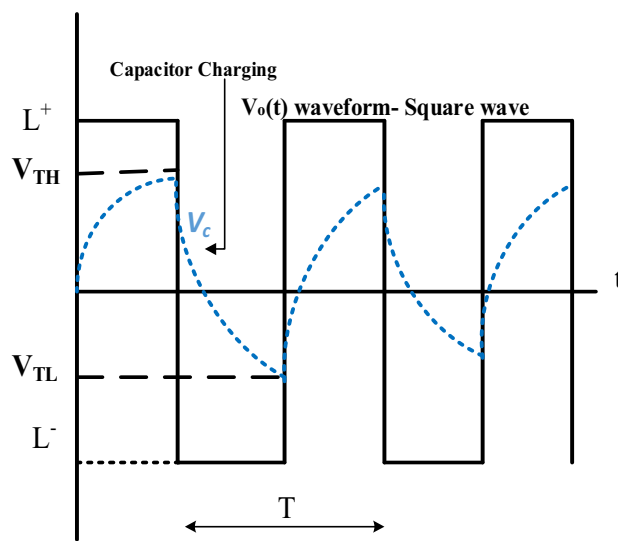


Fig. 5 Specimen waveform of the proposed design

$$q = C \cdot V_{DD}(1 - e^{-t/RC}) - \lambda \cdot C \cdot V_{DD} \cdot e^{-t/RC} \tag{7}$$

Now, Considering the Fig. 5, when the charging voltage switches from one cycle to another, a change occurs at the extreme points of V_{TH} and V_{TL} and surely the time $t=T/2$ for the particular squarewave and this particular change can be mathematically drafted in the Eq. 7 viz.

$$-\lambda \cdot C \cdot V_{DD} = C \cdot V_{DD}(1 - e^{-T/2RC}) - \lambda \cdot C \cdot V_{DD} \cdot e^{-T/2RC} \tag{8}$$

Solving above equation for Time period T, we have the following equation;

$$T = 2R_1 C \ln \frac{1 + \lambda}{1 - \lambda} \tag{9}$$

Equation 8 represents the overall time period function of the circuit design to achieve behavior of square wave generator.

4 Simulation results of the proposed square wave generator

The results obtained from simulation study of the proposed circuit were quite adequate and satisfying in anticipation with the theoretical ones. Various types of analytical results were observed on the Cosmos Scope (C-Scope) tool provided by the Hspice tool from Avant. 45 nm bulk cmos modelling parameters [44] were used to simulate the implemented translinear circuit employing MOS transistors. Figure 6 is the output waveform of the circuit with overshoot 0.086% and undershoot of 0.0057348 (nearly 3.0277%). Hence depict the exemplary linearity and

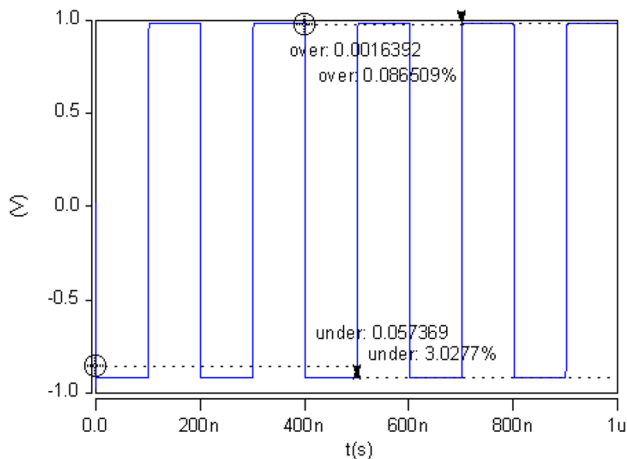


Fig. 6 Output waveform of the proposed square wave generator with the over and undershoot compressions

consistency of the square waveform. A detailed analysis of the proposed circuit provided in the Fig. 4 was done, including the decision making analysis.

Figure 7 observed output electrical properties of the proposed circuit in Fig. 4: Rise time 666.97 ps and fall time 79.32 ps, Slew rate 2.1794 g, Period of one cycle is 200 ns, Frequency of 4.999 MHz, Duty cycle 0.49552 s, Pulse width 99.105 nm. Mean 0.14889, Median 0.52534, Range 1.9601 and Standard deviation 0.84512 (Table 2).

Figures 8 and 9 represent the histograms of the square wave generator in two forms. Former one pointed at Fig. 8 has number of bins = 20, with the advantage of having impact with cumulative and normalising functions than the latter one shown in Fig. 9. Apart from this, Frequency Fourier transform analysis of the Fig. 4 is done here. FFT was done using the time increment linear/logarithmic, waveform view line/spectral, sampling frequency – 2.08 GHz and window function using various scheme. Few parameters like total harmonic distortion-THD, signal to noise ratio-SNR, Signal to noise and distortion ratio-SINAD were calculated for the proposed circuit. Phase and the Noise Plots of the circuit at the Fig. 4, have been analyzed using hann,

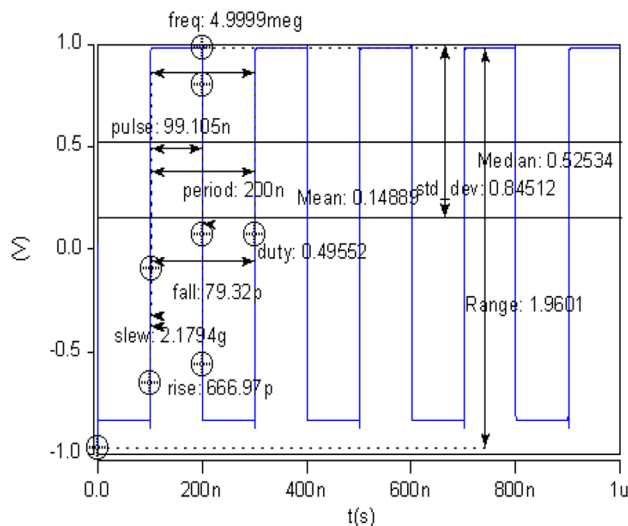


Fig. 7 Detailed analysis plot of the proposed circuit

Table 2 W/L of MOSFET'S used to implement proposed design

Transistor no.	Width (micrometer)	Length (micrometer)
Mn ₁ , Mn ₂ , Mp ₅ , Mp	0.5 u	0.1 u
Mn ₈ , Mn ₁₀ , Mp ₁₃	0.5 u	0.1 u
Mp ₃ , Mn ₄ , Mn ₆ , Mp ₉ , Mp ₁₁ , Mn ₁₂	2.5 u	0.5 u

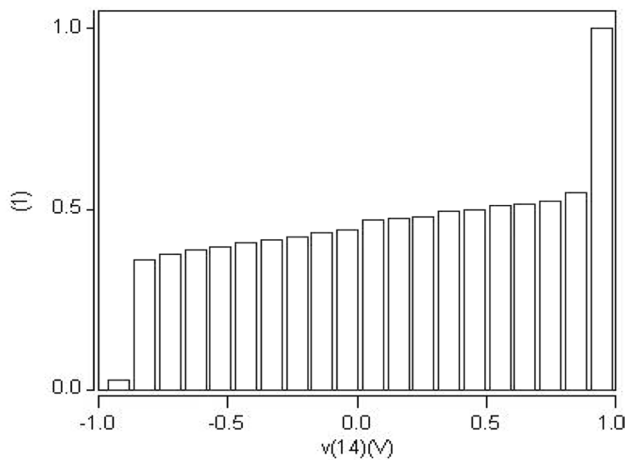


Fig. 8 Effective histogram of the proposed design

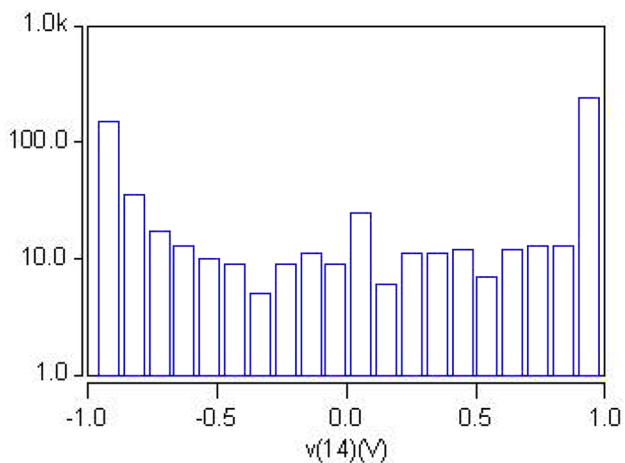


Fig. 9 Actual histogram of the proposed design

hamming, Blackman, flat top, cosine, rectangular and Bartlett window schemes. A quick overview of the results has also been summarized in the Table 3 below. For a total of 10 harmonics Fourier components at output (V(14)-O/P node) were observed with overall dc component finally

figured at 9.39E-02 and overall total harmonic distortion 43.2281%.

In addition to the above analysis, several other circuit response have also used to analyse the behaviour of the proposed circuit. Continuity as well as the linearity of the design in Fig. 4 can be well deprived form these plots.

Detailed 1st order Best Fit Pareto Plot of the Proposed Circuit is signposted in the above plot involving the statistical measurement with comprehensive decision making analysis for the overall extreme performance of the various nodes as well the device/electrical properties for the expanded view (*Translinear circuit Topology*) of the proposed design presented in Fig. 4. In this Plot, X1 stands for the major active element(CCCII +), V(13) is the voltage at the node Y, V(12) represents voltage at node X and V(14) is the output voltage at node Z. TPOWER is the total power of the circuit, i(vss) and i(vdd) are the drain and source currents. x1[v(5), v(3), v(4), v(8), v(7) and v(10)] are the voltages across the mos transistors as per the nomenclature adopted for the proposed circuit topology in the Fig. 5.

5 Pre and post layout designs of the proposed circuit

Layout simulations were carried out using Tanner tool (*L-Edit-v16* and *S-Edit-v16*). A good agreement of satisfying results in both of the layouts and the performed spice simulations was seen. The width (W) and length (L) of the MOS were kept under the bounds of the Tanner Tool. Generic 250 nm device parameters were used for the prelayout simulation with $W = 1.5 \mu$ and $L = 250 \text{ n}$. Further, a simplified post layout simulation has been put before the readers for better understanding, with MOS width of 450 nm and length of 250 nm. Lastly, Simulations were observed out, using *layout extraction method* (Figs. 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22 and 23).

Table 3 Comparative numerical analysis of THD, SNR and SINAD

Parameter	Blackman response	Hamming response	Rectangular response	Flat top response	Cosine response	Bartlett response
THD	26.957	28.581	58.156	25.91	26.301	28.958
SNR	-26.957	-28.581	-58.156	25.91	-26.301	-28.958
SINAD	-26.957	-28.581	-58.156	25.91	-26.301	-28.958

The detailed comparative summary of the Total harmonic distortion (THD), Signal to Noise ratio (SNR) and Signal to Noise and Distortion ratio (SINAD) is shown in the Table 3 Above

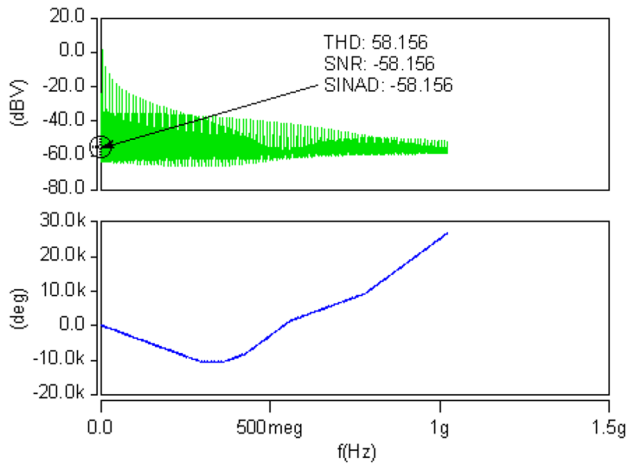


Fig. 10 FFT analysis using rectangular window scheme

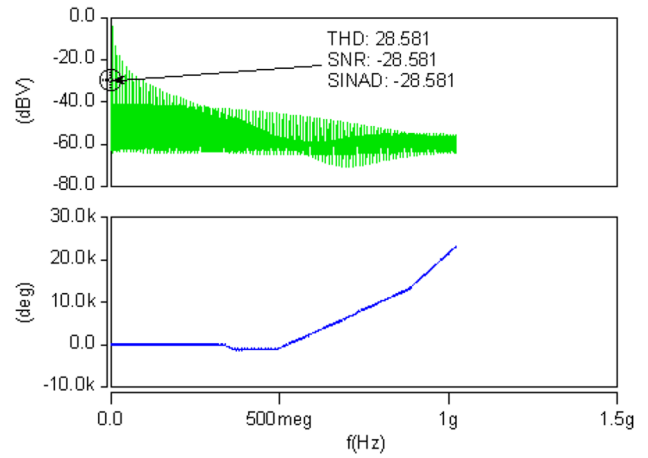


Fig. 13 FFT analysis using Hamming window scheme

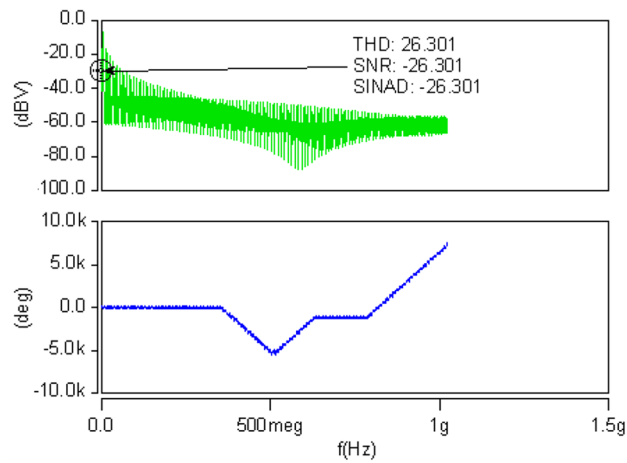


Fig. 11 FFT analysis using Blackman window scheme

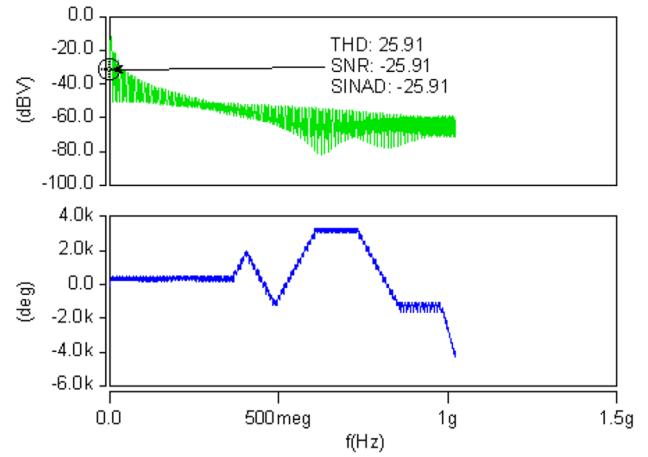


Fig. 14 FFT analysis using flatop window scheme

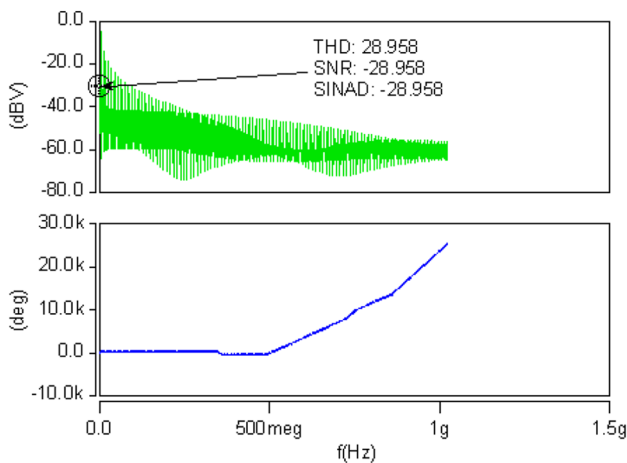


Fig. 12 FFT analysis using Bartlett window scheme

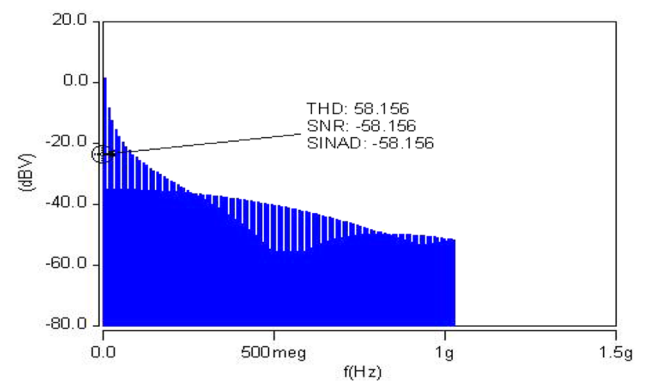


Fig. 15 Logarithmic plot using rectangular window scheme

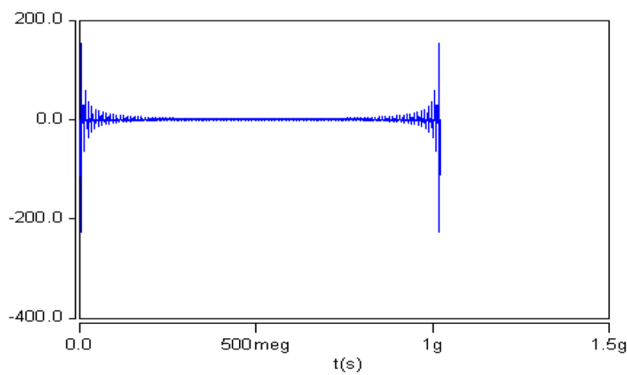


Fig. 16 IFFT plot of the proposed circuit

the realisation. Figure 24 shows the hardware schematic of the AD844 based square wave generator circuit.

Comparison of simulated and measured results The setup in the figure X as well as the simulated results of the Fig. 4, conclude the working of the circuits for wide range of frequencies up to the megahertz range (~ 4 MHz). However, a large variation of the supply voltage was seen in between the simulated and the measured circuits. AD844 based CCCII requires a supply voltage of not less than 5 V, whereas the simulated circuit runs only on a supply voltage of 1 V. Nevertheless, it is better to mention, that the layouts presented in the study have close comparison with the simulated results (Fig. 25).

6 Hardware implementation of the proposed circuit using conventional ad844 ic

Commercially available CCII in the form of AD844 IC was used to realise the proposed square wave generator. Two AD844 IC's were used as a single CCCII IC, for carrying out

7 Evaluation of the pre and presented square wave generator circuits

Circuits available in the literature possess the clarity as well as the conventional Industrial perspective too. In addition, the presented circuits in literature edify satisfying results,

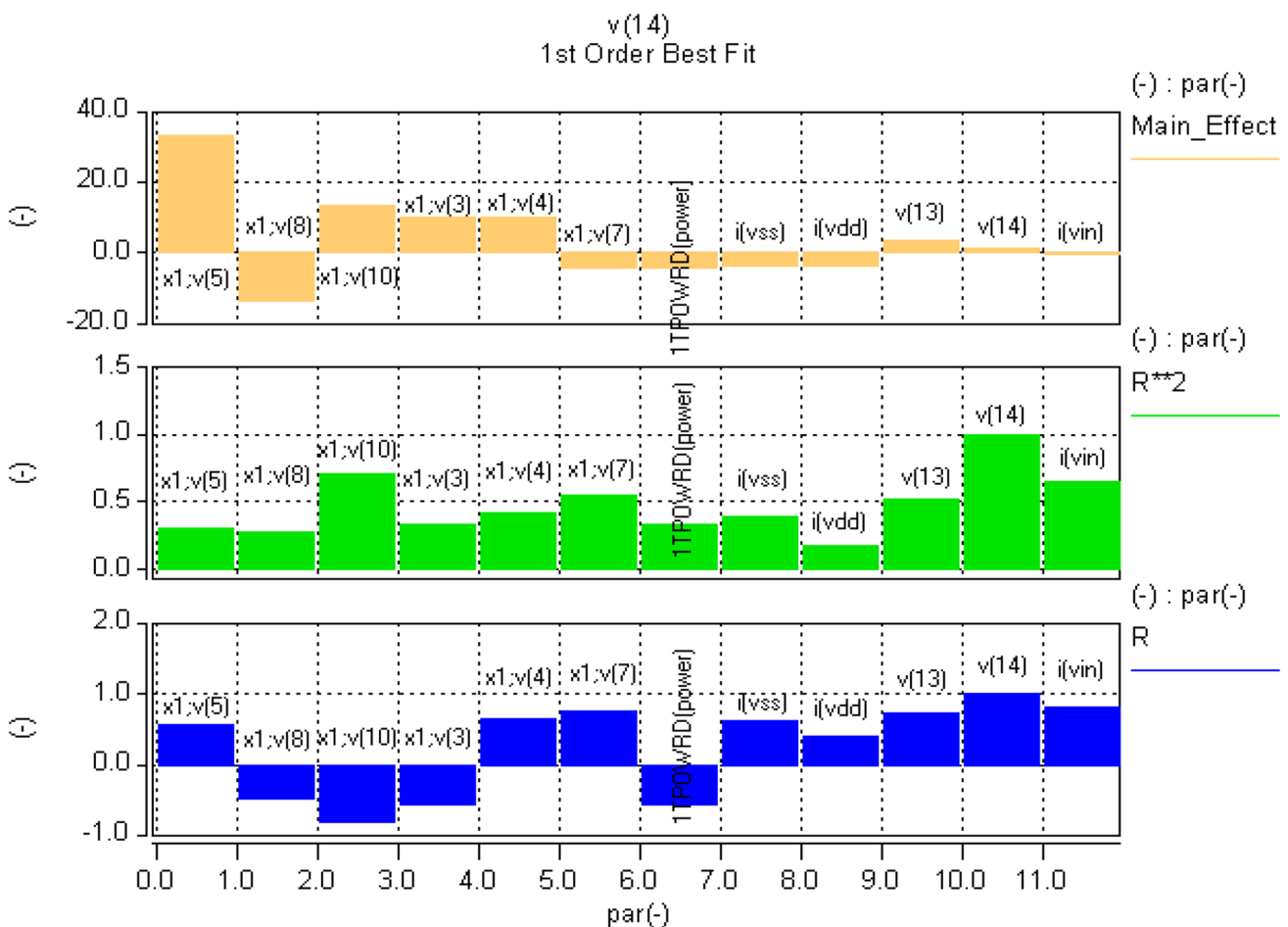


Fig. 17 Pareto plot of proposed circuit

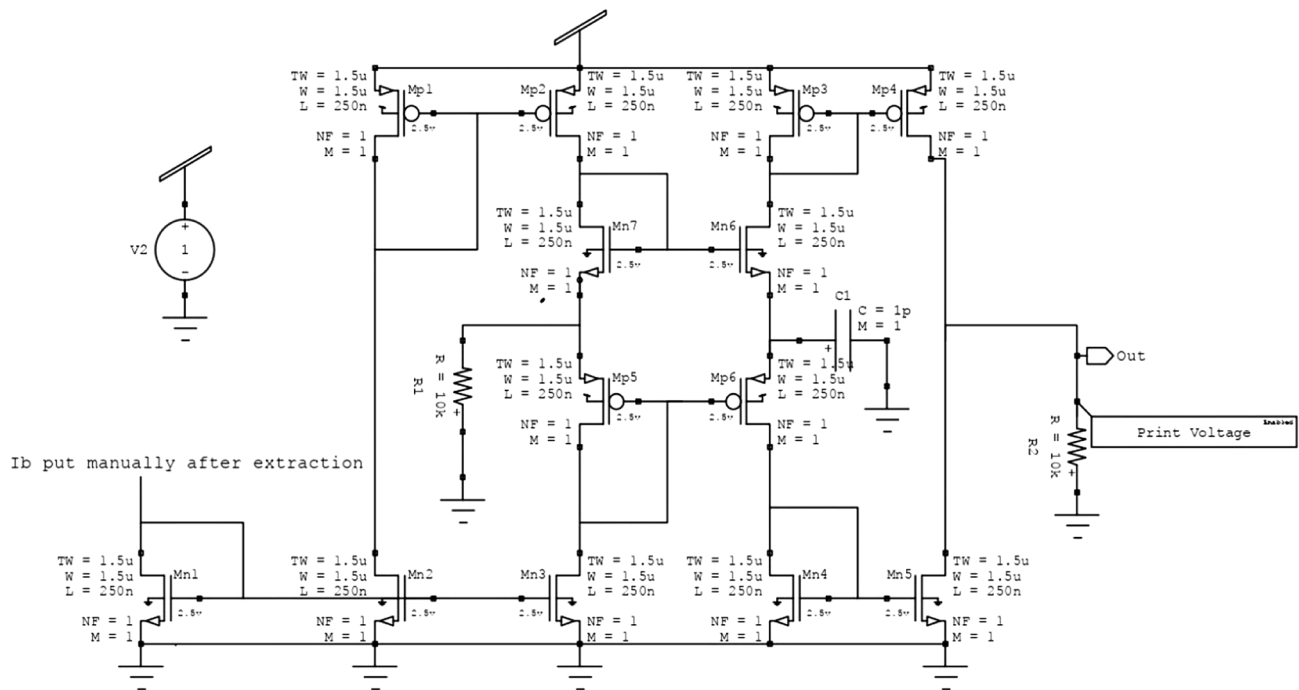


Fig. 18 Prelayout of the proposed circuit in S-Edit-v16 Mentor graphics Tool

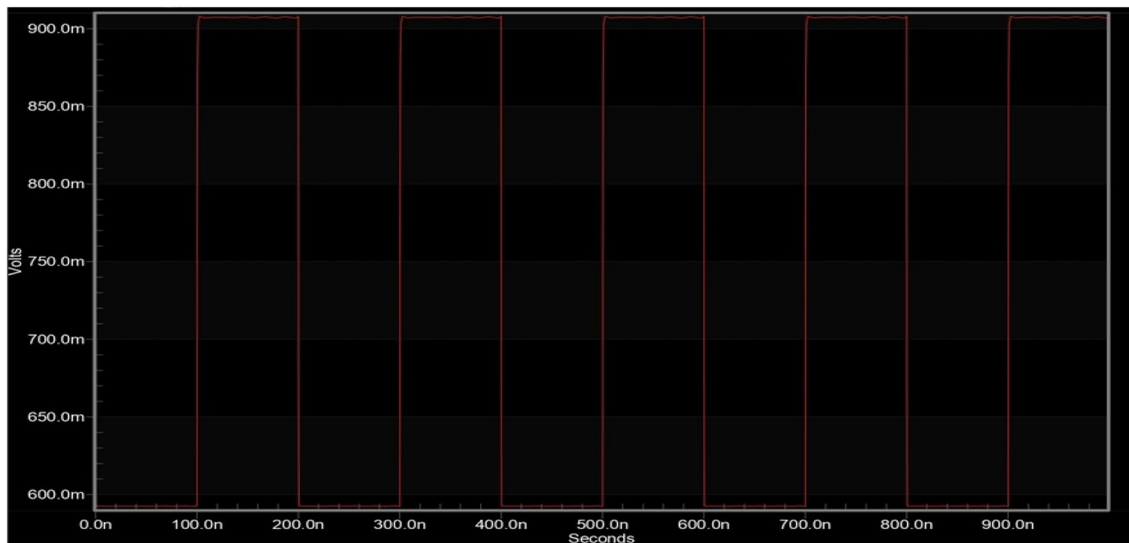


Fig. 19 Simulation O/P of the prelayout of the Fig. 18

however in the modern Industrial era of nanotechnology, an intense focus on chip Area and Power is kept whilst designing circuits. Circuits presented in the literature [13] [28] [29] have the drawback of having more number of active and passive elements than the presented in Fig. 4. Moreover, circuits presented at [16–22] [26] are lagging the grounding feature of passive elements. The striking feature of our work is the implementation of the square wave generator using the

translinear circuit scheme of CCCII+ (with a single CCCII+ as active device and all three passive elements grounded). To the author’s prior knowledge, the presented circuit scheme is not available in the literature till now. Circuit designed in Fig. 5, facilitates low power, low voltage terminology, high slew rate, expected to give advanced performance at higher frequencies and first of its kind implemented in the ultra-deep submicron technology. Another thing that

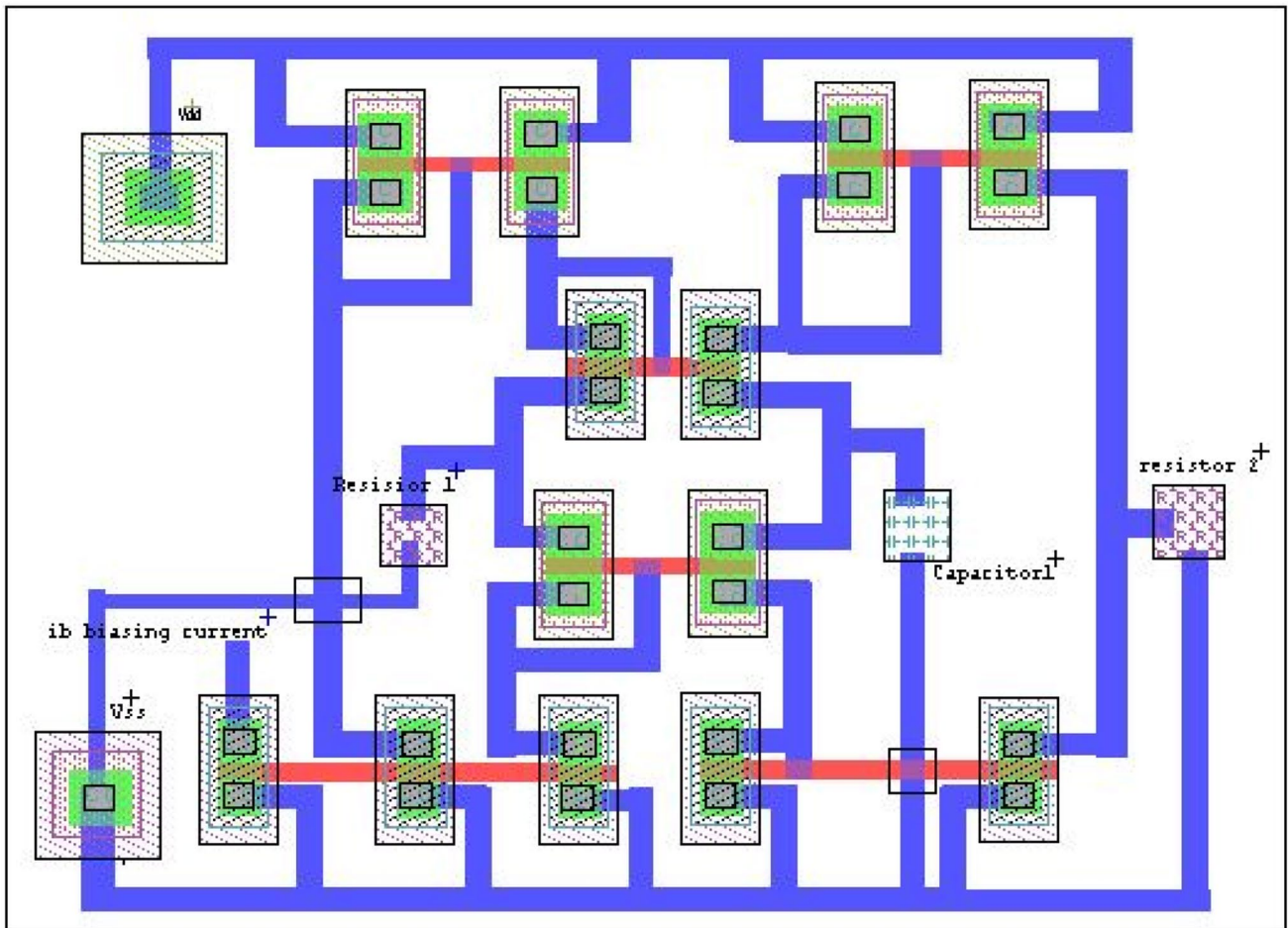


Fig. 20 Post layout of the proposed circuit in L-Edit-v16 Mentor graphics Tool

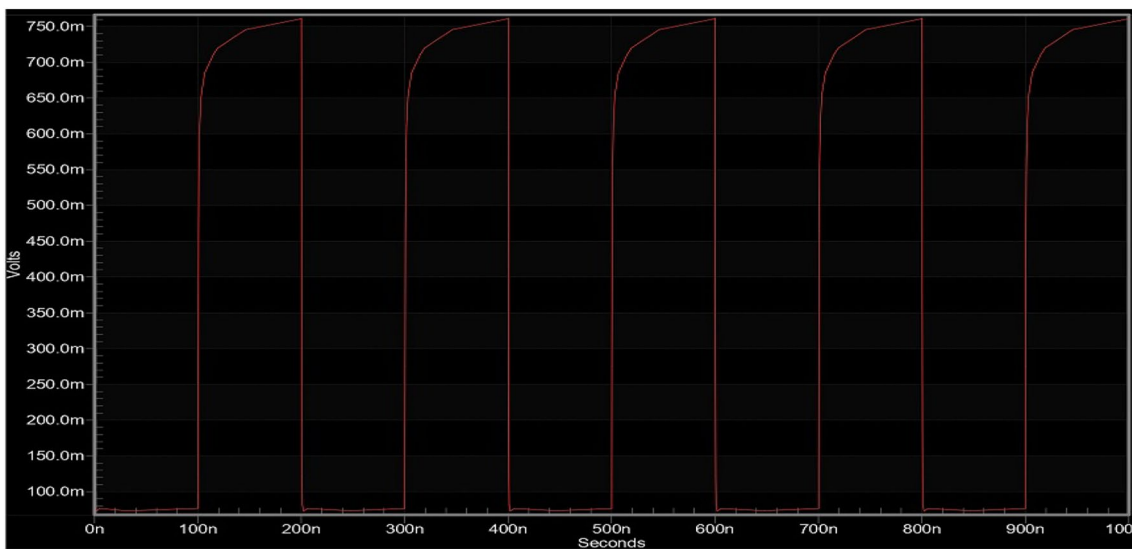


Fig. 21 Simulation O/P of the Post layout of the Figure x

circuit.

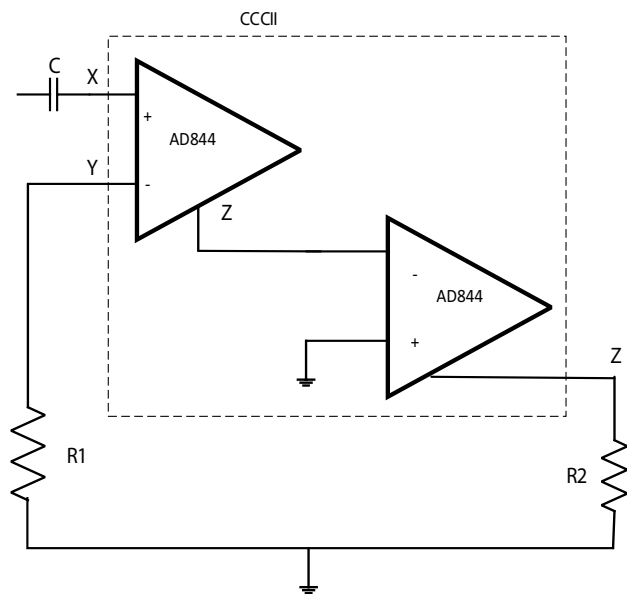


Fig. 22 Hardware setup of the proposed circuit

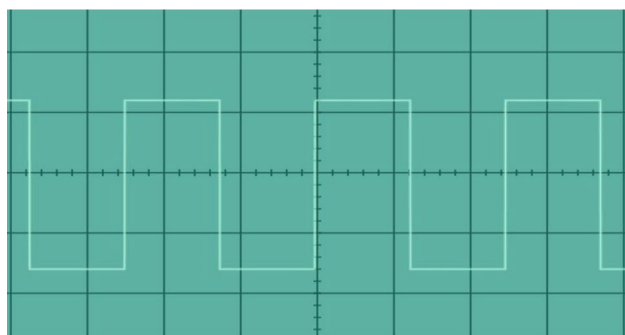


Fig. 23 Waveform (Seconds/Division: 1 ms and Volts/Division: 5 V) on the oscilloscope of Figure X

differentiates this circuit scheme from the literature, is the use of Minimum number of MOS transistors occupied in the translinear circuit adopted. Total power consumption of the circuit is $600 \mu\text{W}$, with $\pm 1 \text{ V}$ rail to rail operating voltages. To the author’s prior knowledge, the circuit (MOS based) presented guarantees the lowermost total power consumption amongst all the circuits presented in literature till date. However, only at [34], circuit presented using BJT’s has extreme low power consumption. The reason behind the fact, that the total power consumption reported at [34] is less than the proposed circuit, is directly due to the implementation of the BJT’s at the *transistor level* for Schmitt trigger device and not used as the *switch* or as active *building blocks*. Further, the application of the BJT and its dominance stem from the use in the particular application and utility. Graphical

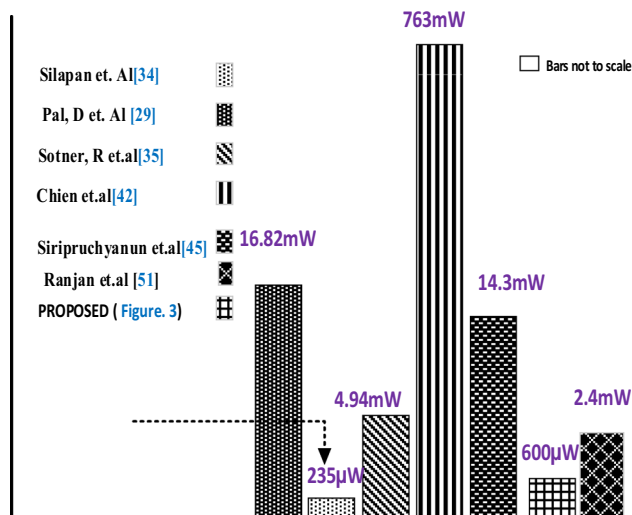


Fig. 24 Figure showing the comparative power consumption of the circuits presented in the literature and the proposed one in the Fig. 3 of this work

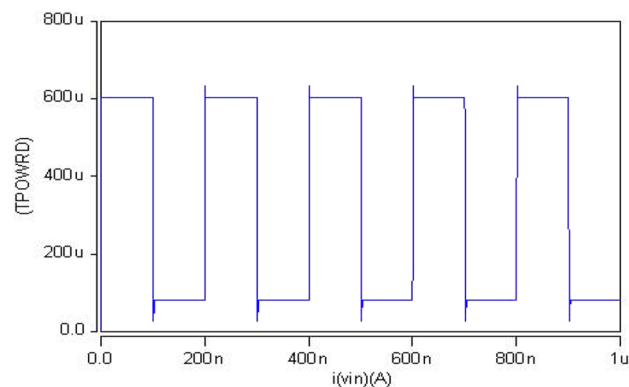


Fig. 25 Total Power Plot of the proposed squarewave circuit

plot of total power consumption of the circuits presented in the literature and the proposed one is shown below in the Fig. 18. To the Authors prior knowledge, the proposed circuit consumes the least power among all other circuits available in the literature. Main and possible reason behind the least power consumption is the implementation of the presented circuit using the 45 nm BSIM predictive modelling technology. Use of deep sub-micron parameters enhances greatly the higher drive as well as the minimization of the leakage current of the circuits.

8 Conclusion and future work

Low voltage and low power square wave generator using CCCII + is presented in this study. The circuit was implemented using a sole capacitor and two resistors. Simulated

and Measured results of the circuit has been also detailed in the manuscript. Apart from the wide simulation analysis, the proposed circuit was also demonstrated practically using commercially available CCII, in the form of AD844 IC. A fair agreement and anticipation of theoretical and practical results was observed. Proposed circuit was passed through high level Pareto analysis with the scope of decision making. Satisfying results were obtained during the whole of the simulation processes. Presented circuit is expected to deliver sophisticated performance than the already existing in the literature. Total power consumption of the circuit is 600 μ W, with ± 1 V rail to rail operating voltages. High frequency application part in the wider areas of electronics and communication are expected to be covered by the presented design. In Future, authors are making efforts to present the extended and enhanced simulations of the pre and post layouts using 45 nm technology parameters with the inclusion of DIE of the proposed circuit from the author's university lab. Finally, a compact and a minaturised device fabricated from a local foundry is also expected to be put before the readers.

Acknowledgements The authors are thankful to the reviewers for their valuable comments.

Compliance with ethical standards

Conflict of interest The author(s) declare that they have no competing interests.

References

- Smith KC, Sedra A (1968) The current conveyor—A new circuit building block. *Proc IEEE* 56(8):1368–1369
- Fabre A et al (1996) High frequency applications based on a new current controlled conveyor. *IEEE Trans Circuits Syst I Fundam Theory Appl* 43(2):82–91
- Smith K, Sedra A (1970) Realization of the Chua family of new nonlinear network elements using the current conveyor. *IEEE Trans Circuit Theory* 17(1):137–139
- Sedra AS, Smith KC (1970) A second-generation current conveyor and its applications. *IEEE Trans Circuit Theory* 17(1):132–134
- Fabre A et al (1996) High frequency applications based on a new current controlled conveyor. *IEEE Trans Circuits Syst I Fundam Theory Appl* 43(2):82–91
- Armağan E, Kuntman H (2013) Configurable frequency agile filter application of balanced differential pair based CCCII circuit in 28 nm process. 2013 IEEE fourth Latin American symposium on circuits and systems (LASCAS). IEEE
- Biolek D et al (2008) Active elements for analog signal processing: classification, review, and new proposals. *Radioengineering* 17(4):15–32
- Yucek T, Arslan H (2009) A survey of spectrum sensing algorithms for cognitive radio applications. *IEEE Commun Surv Tutor* 11(1):116–130
- Stern E et al (2007) Label-free immunodetection with CMOS-compatible semiconducting nanowires. *Nature* 445(7127):519
- Berner B, Dunn TC, Farinas KC, Garrison MD, Kurnik RT, Lesho MJ, Potts RO, Tamada JA, Tierney MJ, Cygnus Inc, (2003). Device for signal processing for measurement of physiological analytes. U.S. Patent 6,595,919
- Biolek D (2003) CDTA-building block for current-mode analog signal processing. *Proc ECCTD* 3:397–400
- Fabre A et al (1996) High frequency applications based on a new current controlled conveyor. *IEEE Trans Circuits Syst I Fundam Theory Appl* 43(2):82–91
- Awad IA (1999) Inverting second generation current conveyors: the missing building blocks, CMOS realizations and applications. *Int J Electron* 86(4):413–432
- Fabre A, Saaid O, Barthelemy H (1995) On the frequency limitations of the circuits based on second generation current conveyors. *Analog Integr Circuits Signal Process* 7(2):113–129
- Fabre A, Barthelemy H (1994) Composite second-generation current conveyor with reduced parasitic resistance. *Electron Lett* 30(5):377–378
- Alzahrer HA, Elwan H, Ismail M (2003) A CMOS fully balanced second-generation current conveyor. *IEEE Trans Circuits Syst II Analog Digital Signal Process* 50(6):278–287
- Abbas Z, Scotti G, Olivieri M (2011) Current controlled current conveyor (CCCI) and application using 65 nm CMOS technology. *World Acad Sci Eng Technol* 55:935–939
- Yasin MY, Gopal B (2011) High frequency oscillator design using a single 45 nm CMOS current controlled current conveyor (CCCI+) with minimum passive components. *Circuits Syst* 2(02):53
- Biolek D et al (2008) Active elements for analog signal processing: classification, review, and new proposals. *Radioengineering* 17(4):15–32
- Gray PR et al. (2001) Analysis and design of analog integrated circuits. Wiley
- Chaisrichaen R, Chipipop B, Sirinaovakul B (2010) CMOS CCCII: structures, characteristics, and considerations. *AEU-Int J Electron Commun* 64(6):540–557
- Wang C, Liu H, Zhao Y (2008) A new current-mode current-controlled universal filter based on CCCII (\pm). *Circuits Syst Signal Process* 27(5):673–682
- Chaisrichaen R, Chipipop B, Sirinaovakul B (2010) CMOS CCCII: structures, characteristics, and considerations. *AEU-Int J Electron Commun* 64(6):540–557
- Ercan H, Alçi M (2013) A new design for a BiCMOS controlled current conveyor. *Elektronika Ir Elektrotechnika* 19(1): 56–60
- Al-Shahrani SM, Al-Gahtani MA (2006) A new polyphase current-mode filter using digitally-programmable CCCII. In: 2006 international conference on microelectronics ICM'06, IEEE
- Yasin MY (2013) A Novel bipolar XOR/XNOR realization using translinear type 2nd generation current controlled current conveyor designed in 45 nm CMOS technology. *Acta Electrotechnica* 54:3–6
- Hou Chun-Li, Shen B (1995) Second-generation current conveyor-based multiphase sinusoidal oscillators. *Int J Electron* 78(2):317–325
- Hou CL, Chien H-C, Lo Y-K (2005) Squarewave generators employing OTRAs. *IEE Proc Circuits Devices Syst* 152(6):718–722
- Pal D, Srinivasulu A, Goswami M (2009) Novel current-mode waveform generator with independent frequency and amplitude control. In: Proceedings of the IEEE international symposium on circuits and systems-2009, Taipei, Taiwan, 24–27, pp. 2946–2949
- Silapan P, Siripruchyanun M (2011) Fully and electronically controllable current-mode Schmitt triggers employing only single MO-CCDTA and their applications. *Analog Integr Circuits Signal Process* 68(1):111–128

31. Ercan H, Tekin SA, Alçı M (2015) Low-voltage low-power multifunction current-controlled conveyor. *Int J Electron* 102(3):444–461
32. Lo Y-K, Chien H-C (2007) Switch-controllable OTRA-based square/triangular waveform generator. *IEEE Trans Circuits Syst II Express Briefs* 54(12):1110–1114
33. Hou CL, Chien H-C, Lo Y-K (2005) Squarewave generators employing OTRAs. *IEE Proc Circuits Devices Syst* 152(6):718–722
34. Silapan P, Siripruchyanun M (2011) Fully and electronically controllable current-mode Schmitt triggers employing only single MO-CCDTA and their applications. *Analog Integr Circuits Signal Process* 68(1):111–128
35. Sotner R, Jerabek J, Herencsar N, Dostal T, Vrba K (2015) Design of Z-copy controlled-gain voltage differencing current conveyor based adjustable functional generator. *Microelectron J* 46(2):143–152
36. Sotner R, Jerabek J, Herencsar N, Lahiri A, Petrzela J, Vrba K (2013) Practical aspects of operation of simple triangular and square wave generator employing diamond transistor and controllable amplifiers. In: *Proceedings of the 36th international conference on telecommunications and signal processing (TSP 2013)*, Rome, Italy, 2–4, pp. 431–435
37. Sotner R, Jerabek J, Herencsar N (2013) Voltage differencing buffered/inverted amplifiers and their applications for signal generation. *Radioengineering* 22(2):490–504
38. Sotner R, Jerabek J, Herencsar N, Prokop R, Vrba K, Petrzela J, Dostal T (2013) Simply adjustable triangular and square wave generator employing controlled gain current and differential voltage amplifier. In: *Proceedings of the 23th international conference radioelektronika*, Pardubice, Czech Republic, 16–17, pp. 109–114
39. Srinivasulu A (2011) A novel current conveyor based Schmitt trigger and its application as a relaxation oscillator. *Int J Circuit Theory Appl* 39(6):679–686
40. Srinivasulu A (2009) Current conveyor-based square-wave generator with tunable grounded resistor/capacitor. In: *Proceedings of the IEEE applied electronics international conference (AEIC 2009)*, Pilsen, Czech Republic, pp 233–236
41. Siripruchyanun M, Wardkein P (2003) A fully independently adjustable integrable simple current controlled oscillator and derivative PWM signal generator. *IEICE Trans Fundam Electron Commun Comput Sci* 86(E12-A):3119–3126
42. Chien H-C (2012) Voltage-controlled dual slope operation square/triangular wave generator and its application as a dual mode operation pulse width modulator employing differential voltage current conveyors. *Microelectron J* 43(12):962–974
43. Vijay V, Srinivasulu A (2017) A novel square wave generator using second-generation differential current conveyor. *Arab J Sci Eng* 42(12):4983–4990
44. Simpson RE (1974) *Introductory electronics for scientists and engineers*. Allyn and Bacon, Boston
45. Chaturvedi B, Kumar A (2018) A novel electronically controlled Schmitt trigger with clockwise and anticlockwise hystereses. *AEU Int J Electron Commun* 89:136–145
46. Siripruchyanun M et al (2016) A Current-mode square/triangular wave generator based on multiple-output VDTAs. *Procedia Comput Sci* 86:152–155
47. Chaturvedi B, Kumar A (2018) A novel linear square/triangular wave generator with tunable duty cycle. *AEU Int J Electron Commun* 84:206–209
48. Kumar A, Chaturvedi B (2017) Novel electronically controlled current-mode Schmitt trigger based on single active element. *AEU Int J Electron Commun* 82:160–166
49. Chaturvedi B, Kumar A (2018) Fully electronically tunable and easily cascadable square/triangular wave generator with duty cycle adjustment. *J Circuits Syst Comput*. <https://doi.org/10.1142/S0218126619501056>
50. Kumar A, Chaturvedi B, Maheshwari S (2017) A fully electronically controllable Schmitt trigger and duty cycle modulated waveform generator. *Int J Circuit Theory Appl* 45(12):2157–2180
51. Ranjan A, Pamu H, Tarunkumar H (2018) A novel Schmitt trigger and its application using a single four terminal floating nullor (FTFN). *Analog Integr Circuits Signal Process* 96(3):455–467
52. De Marcellis A, Di Carlo C, Ferri G, Stornelli V (2013) A CCII-based wide frequency range square waveform generator. *Int J Circuit Theory Appl*, ISSN, pp 0098–9886
53. De Marcellis A et al (2009) A novel low-voltage low-power fully differential voltage and current gained CCII for floating impedance simulations. *Microelectron J* 40(1):20–25
54. Stornelli V, Ferri G (2014) A single current conveyor-based low voltage low power bootstrap circuit for electrocardiography and electroencephalography acquisition systems. *Analog Integr Circuits Signal Process* 79:171–175. <https://doi.org/10.1007/s10470-013-0252-2>
55. Amlık S et al. (2015) A CCII-based wide frequency range square/triangular wave generator. In: *2015 IEEE 2nd international conference on recent trends in information systems (retis)*, Date of Conference: 9–11 July 2. <https://doi.org/10.1109/retis.2015.7232920>
56. Ercan H, Alci M (2013) A new design for a BiCMOS controlled current conveyor. *Elektronika ir Elektrotechnika* 19(1):56–61
57. Fabre A, Saaid O, Wiest F, Bouchron C (1995) Current controlled bandpass filter based on translinear conveyors. *Electron Lett* 31(20):1727–1728
58. Chaisricharoen R, Chipipop B, Sirinaovakul B (2010) CMOS CCCII: structures, characteristics, and considerations. *Int J Electron Commun* 64:540–557
59. Yuçe E (2008) Design of a simple current-mode multiplier topology using a single CCCII+. *IEEE Trans Instr Meas* 57(3):631–637. <https://doi.org/10.1109/TIM.2007.910112>
60. Zahiruddin S, Srinivasulu A (2015) A high frequency tunable sinusoidal oscillator using single CCCII+. In: *Proceedings of IEEE international conference on control, instrumentation, communication & computational technologies*, Kumaracoil, India, 18th and 19th December, pp 462–465. <https://doi.org/10.1109/iccict.2015.7475323>
61. <http://ptm.asu.edu>

Publisher's Note Springer Nature remains neutral with regard to jurisdictional claims in published maps and institutional affiliations.